Examiner-Initiated Interview Summary	Application No.	Applicant(s)
	10/721,673	QIN ET AL.
	Examiner	Art Unit
	Phallaka Kik	2825
All Participants:	Status of Application: pe	ending
(1) <u>Phallaka Kik</u> .	(3)	
(2) <u>Thomas Chan (Reg. No. 51,543)</u> .	(4)	
Date of Interview: 10 April 2006	Time: <u>4:02PM</u>	
Type of Interview: ☐ Telephonic ☐ Video Conference ☐ Personal (Copy given to: ☐ Applicant ☐ A Exhibit Shown or Demonstrated: ☐ Yes ☐ No If Yes, provide a brief description:	pplicant's representative)	
Part I.	·	
Rejection(s) discussed:		
Claims discussed: 1-70		
Prior art documents discussed: None		
Part II.		
SUBSTANCE OF INTERVIEW DESCRIBING THE G	SENERAL NATURE OF WHAT WA	S DISCUSSED:
Part III.		
 □ It is not necessary for applicant to provide a sepa directly resulted in the allowance of the applicatio of the interview in the Notice of Allowability. □ It is not necessary for applicant to provide a sepa did not result in resolution of all issues. A brief sur 	 The examiner will provide a writter trate record of the substance of the 	ten summary of the substance interview, since the interview
•		
Bhallab Mic		
(Examiner/SPE Signature) (App	licant/Applicant's Representative S	ignature – if appropriate)

Continuation of Substance of Interview including description of the general nature of what was discussed: The Examiner left on Applicant Representative's voice message machine on 4/5/2005 with a restriction requirement for inventions group I, claims 1-62,70 drawn to method/comptuer programmed system/computer executable software code for transforming a circuti from a first topology, classified in 716/3; group II, claims 63-67 drawn to a method of transforming a circuit from a first topology to a reduced toplogy involving reducing the circuit elements in a bottom-up fashion from the neaf nodes to the root of the tree-like topological approximation that was generated, classified in 716/3; group III, claim 68, directed to a method of reducing capacitors within a circuit topology involving moving and merging capactiors identified associated with particular connections to the transistor drain or source node, classified in 716/2; group IV, claim 69, drawn to a method of reducing nodes within a circuit topology involving merging nodes P1 and P2 into one node if P1 and P2 satisfy the particular conditions, classified in 716/2; wherein the inventions are related to each other at least as subcombinations disclosed as usuable together but could have separate utility, and wherein inventions would require different search; related processes; and combination and subcombinations. On April 10, 2006, Applicant's Representative returned the Examiner's telephone call and requested until Wednesday April 12,2006 to consult with Applicant for the election; however, as of April 14, 2006, Applicant's Representative has not contacted the Examiner to elect the invention to prosecute. Accordingly, a written restriction will be given to give Applicant sufficient time to make the decision..